Electrochemical Pore Formation in InP: Understanding and Controlling Pore Morphology

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Abstract

Pores formed anodically in InP at different temperatures, electrolyte (KOH) concentrations, carrier concentrations and current densities exhibit significant pore width variations. The pore width decreases as the temperature, carrier concentration or current density are increased. The pore width also decreases when the KOH concentration is increased up to 9 mol dm^{-3}, but increases slightly as the concentration is increased further. These pore width variations are explained by a three-step model for pore formation based on competition in kinetics between the different steps in the etching mechanism. The variation of pore width with current density is explained explicitly in terms of the crystallographic etching mechanism and this is supported by observation of the different crystallographic features of the pore cross section at different current densities.

Introduction

Electrochemically formed porous semiconductors have received considerable research attention and a wide range of different porous structures can now be produced in a variety of different semiconductors and electrolytes. Although the formation of porous silicon in HF has long been known,[1-4] the discovery of visible luminescence from porous silicon[5] led to a significant increase in research in the formation of porosity in other semiconductors. The list of semiconductors that can now be rendered porous electrochemically includes germanium,[6-8] GaP, [9-11] InP,[12-17] GaAs,[18-22] GaN,[23-25] and many others. A range of different porous structures can be obtained in these semiconductors by variation of electrolyte type and concentration,[14, 26] carrier concentration and substrate orientation,[27, 28] as well as the current density or potential at which the porous structures are formed.[29, 30]

This wide range of porous structures have most often been characterised in terms of their morphology.[4] Most anodically formed porous layers can be characterised by a well-defined average pore width and pore wall thickness.[2] Pores will also often exhibit a specific cross section[31-33] and grow in a particular direction; either crystallographically oriented[2, 34] or aligned to the source of holes.[12, 22, 35] A number of theories have been proposed[2-4, 33, 35-38] to explain the wide range of pore morphologies that have been observed with various semiconductor/electrolyte combinations.

Porous InP is typically formed in acidic, halide containing electrolytes such as HCl.[12, 14, 29] At certain potentials the pores grow along specific directions[39] and are said to be

crystallographically oriented (CO). At higher potentials, pores appear to grow in the general direction of current flow[14, 29] and are said to be current-line oriented (CLO). The ability to switch between these two pore morphologies just by varying the anodization potential has led to considerable interest in the formation of porous InP and its possible applications.

In our group, we have demonstrated the formation of porous InP in KOH electrolytes in the concentration range 1-17 mol dm^{-3}.[17, 40, 41] We have previously shown that pores emerge from pits in the electrode surface[42] and grow and branch along the <111>A crystallographic directions forming tetrahedral porous domains.[34, 39] We have also recently proposed a model for the propagation of crystallographically oriented pores in III-V semiconductors based on competition in kinetics between hole diffusion and electrochemical reaction.[33] In this paper, the effect of temperature, electrolyte concentration, carrier concentration and current density on the morphology of anodically formed pores in InP will be explored. It will be shown that the pore width is strongly influenced by the kinetics of the electrochemical reaction at the pore tip, as well as the nature of the crystallographic etching mechanism as predicted by our model.

Experimental

Wafers were monocrystalline, sulfur-doped, n-type indium phosphide (n-InP) grown by the liquid-encapsulated Czochralski (LEC) method and supplied by Sumitomo Electric. They were polished on one side and had a surface orientation of (100) and had carrier concentrations in the range $3–7 \times 10^{18}$ cm^{-3}. To fabricate working electrodes, wafers were cleaved into coupons along the natural {011} cleavage planes. Ohmic contact was made by alloying indium to the back of a coupon; the back and the cleaved edges were then isolated from the electrolyte by means of a suitable varnish. The electrode area was typically 0.2 cm^2. Prior to immersion in the electrolyte, the working electrode was immersed in a piranha etchant (3:1:1 H_2SO_4:H_2O_2:H_2O) for 4 minutes and then rinsed with deionized water.

Anodization was carried out in aqueous KOH electrolytes in the absence of light using either a linear potential sweep (LPS) at 2.5 mV s^{-1} or a constant current. The temperature of each experiment was kept constant by performing the anodization in a cell housed within a thermostatic water bath. A conventional three-electrode cell configuration was used, employing a platinum counter electrode and a saturated calomel electrode (SCE) to which all potentials are referenced. A CH Instruments Model 650A Electrochemical Workstation interfaced to a Personal Computer (PC) was employed for cell parameter control and for data acquisition. Cleaved $(0\bar{1}1)$ cross sections and the (100) surface of electrodes were examined using a Hitachi S-4800 field-emission scanning electron microscope (FE SEM) operating at 5 kV.

Results and Discussion

Variation of Pore Width with Carrier Concentration

To study the factors effecting pore morphology, porous InP layers were formed under a range of different conditions. Figure 1 shows a number of linear sweep voltammograms (LSVs) for the anodization of n-InP samples with three different carrier concentrations in 5 mol dm^{-3} KOH at room temperature. The observed current peaks are due to the localised dissolution of the InP surface, creating pores which penetrate deep below the surface and propagate along the <111>A directions.[34] Figure 2 is an SEM image showing some of the general features of crsytallographically oriented (CO) pore etching in InP. (Under certain conditions, pore etching can be made to deviate from crystallogrphically defined directions and become aligned with the source of carriers (holes) forming current-line oriented (CLO) pores.[12, 29, 41] This type of etching is not dealt with in this paper.) Typically, two pores originate from each surface pit and propagate along <111>A directions. As these pores propagate, more pores can be seen to branch off in the remaining <111>A directions forming a porous domain in which every pore is connected to the original surface pit.[34]

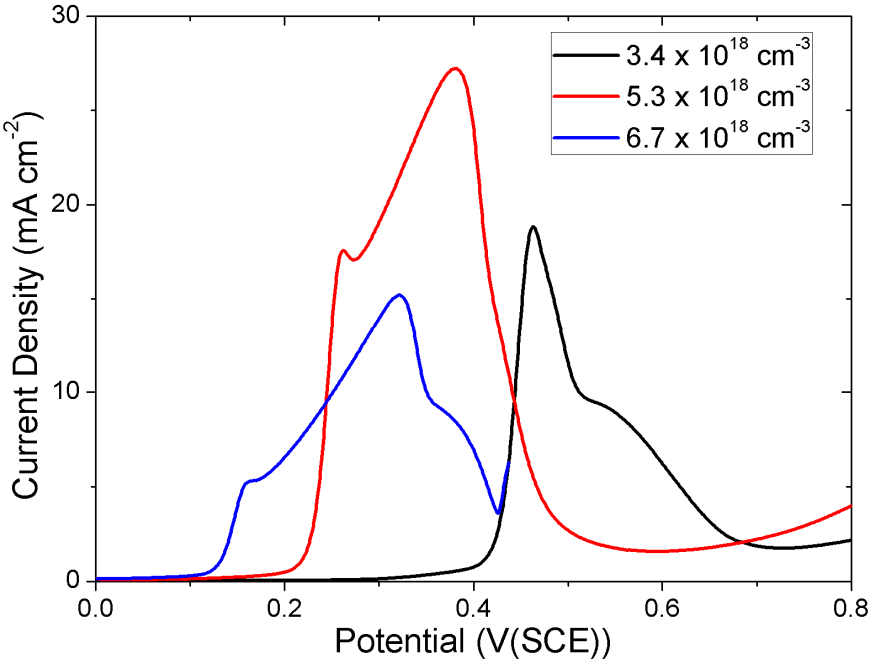


Figure 1. LSVs of n-InP performed for three different carrier concentrations at a scan rate of 2.5 mV s^{-1} at room temperature in 5 mol dm^{-3} KOH.

For the LSVs in Fig. 1, the number and magnitude of the current peaks changes with carrier concentration. We have previously described how each feature of the LSV corresponds to a particular stage during the formation of a porous layer at the InP surface.[27, 34, 43] Here we shall mention only the pitting potential; so called because it is the potential at which etch pits start to appear on the electrode surface.[42] On an LSV, the pitting potential is the potential at which a significant current begins to flow through the electrode. For n-type semiconductors anodised in the dark, no current will flow at lower potentials because the surface is depleted of carriers. The holes necessary for the electrochemical reaction can only be supplied by tunneling across the depletion layer at

the surface,[33, 44] which requires a high electric field at the surface. Therefore a minimum threshold potential (*i.e.* the pitting potential) must be exceeded before a significant current can flow. In Fig. 1, the pitting potential increases from ~0.16 V to ~0.32 V as the carrier concentration is decreased from ~6.7 to ~3.4 x 10^{18} cm^{-3}. The increase in the pitting potential is likely due to the increase in depletion layer thickness x_{sc} that is expected as carrier concentration is decreased. This lowers the energy barrier for the tunnelling of holes to the semiconductor surface.

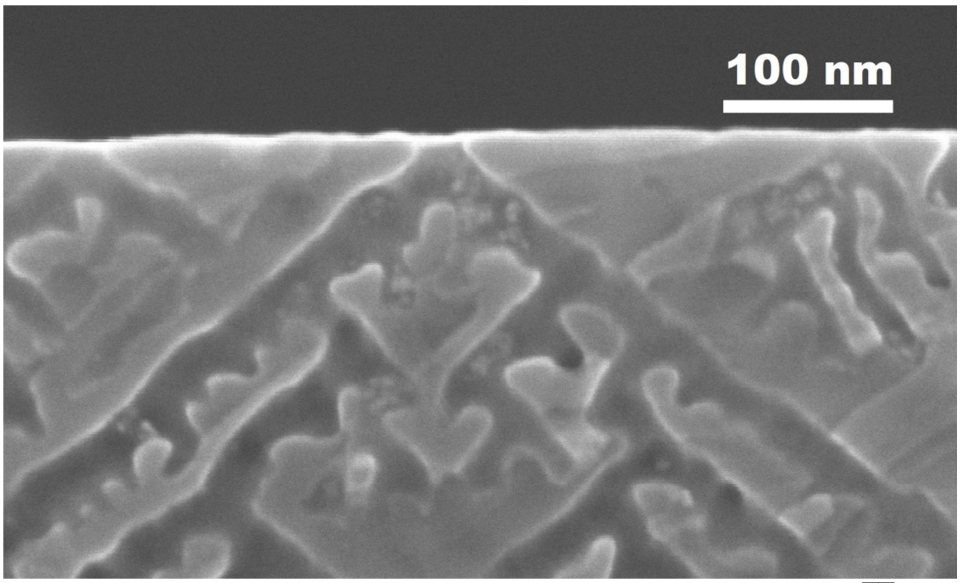


Figure 2. Cross Sectional SEM micrograph of the surface region of the $(0\overline{1}\overline{1})$ plane of an n-InP sample galvanostatically anodised at 5 mA cm^{-2} in 5 mol dm^{-3} KOH. An etch pit can be seen penetrating the InP surface forming two pores which propagate along <111>A directions and exhibit regular branching in those directions.

The average pore width (determined from the mean value of ~90 SEM measurements of pores on the $(0\overline{1}\overline{1})$ cross section) of each InP sample was measured and the results are plotted in Fig. 3. The pore width decreases from 30 to 19 nm as the carrier concentration is increased from ~3.4 to ~6.7 x 10^{18} cm^{-3}. A decrease in pore width with carrier concentration has also been noted before in Si.[37, 45] This variation in pore width with carrier concentration can be understood by considering the electric field enhancement that occurs at the curved surface of a pore tip. According to Zhang,[44] the electric field at the surface is inversely related to r_0/x_{sc} where r_0 is the radius of curvature at the pore tip. (Note: x_{sc} is the depleation layer thickness at a flat surface.) At low carrier concentrations, x_{sc} is larger and so a larger value of r_0 will suffice to achieve the electric field necessary for tunnelling to occur. This allows tunnelling to occur over a wide region of the pore tip. As a result, etching can occur over a wide region leading to relatively wide pores. At higher carrier concentrations however, x_{sc} is smaller and so the value of r_0 necessary to achieve tunnelling must be correspondingly smaller. This results in hole supply being confined to the sharpest region of the pore tip leading to etching occurring over a smaller area. This results in the expected decrease in pore width with increasing carrier concentration shown in Fig. 3.

Though the variation in pore width with carrier concentration can be explained by considering only the variation of the curvature of the pore tip, there are many other factors which affect pore width which require a more comprehensive explanation.

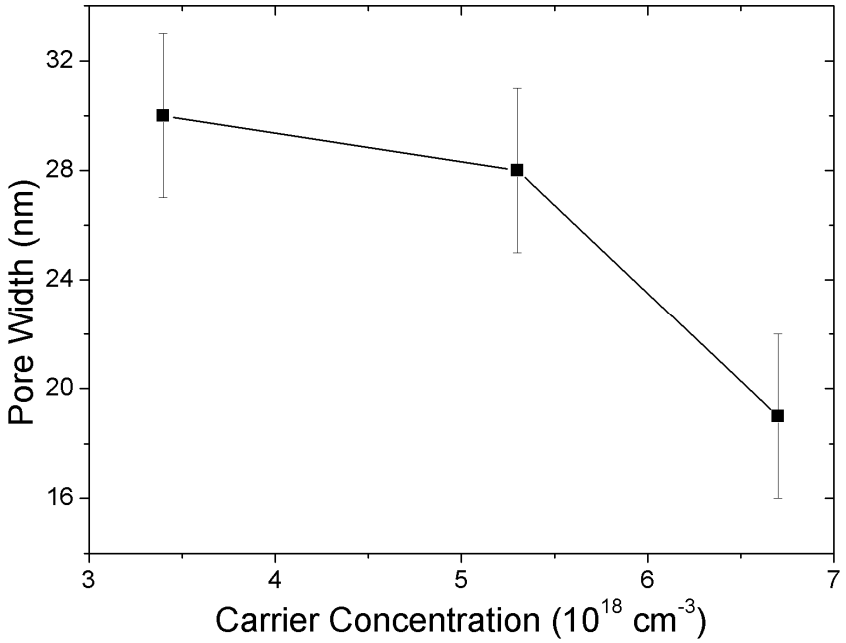


Figure 3. Plot of pore width against carrier concentration for porous InP layers formed by LPS at 2.5 mV s^{-1} in 5 mol dm^{-3} KOH at room temperature as in Fig. 1.

Variation of pore width with temperature, KOH Concentration and Current Density

InP porous layers were formed at different temperatures by linear potential sweep (LPS) in 9 mol dm^{-3} KOH. As before, the average pore width of each sample was measured and the results are plotted in Fig. 4. The average pore width decreases from 38 to 26 nm as the temperature is increased by 40 K. This variation cannot be explained in terms of changing depletion layer thickness as in the case of the variation of pore width with carrier concentration.

Porous layers were also formed at a range of KOH concentrations by LPS at 25°C. The variation in pore width with KOH concentration is plotted in Fig. 5. The pore width decreases from 41 to 31 nm as the KOH concentration is increased from 2.5 to 9 mol dm^{-3}. Above 9 mol dm^{-3} however, the opposite trend is observed: pore width increases to 33 nm as the KOH concentration is increased to 17 mol dm^{-3}. A decrease in pore width with increasing electrolyte concentration has been noted previously for InP in KOH[17, 46] and for Si anodised in HF.[47]

Since all of these porous layers (those anodised at different carrier concentrations, temperatures and different KOH concentrations) were formed by LPS, the current during each experiment was not controlled and generally varied with both temperature and KOH concentration just as it varied for carrier concentration (see Fig. 1). It has been reported before that pore width can vary with current density.[44,48-50] To see if the pore width variation could be explained in terms of current density variation, a number of InP porous layers were formed galvanostatically at different values of current density. As before these samples all had their average pore width measured using SEM and the results are plotted in Fig. 6. Pore width can be seen to decrease from 49 nm at 1 mA cm^{-2} to 27 nm at 20 mA cm^{-2}.

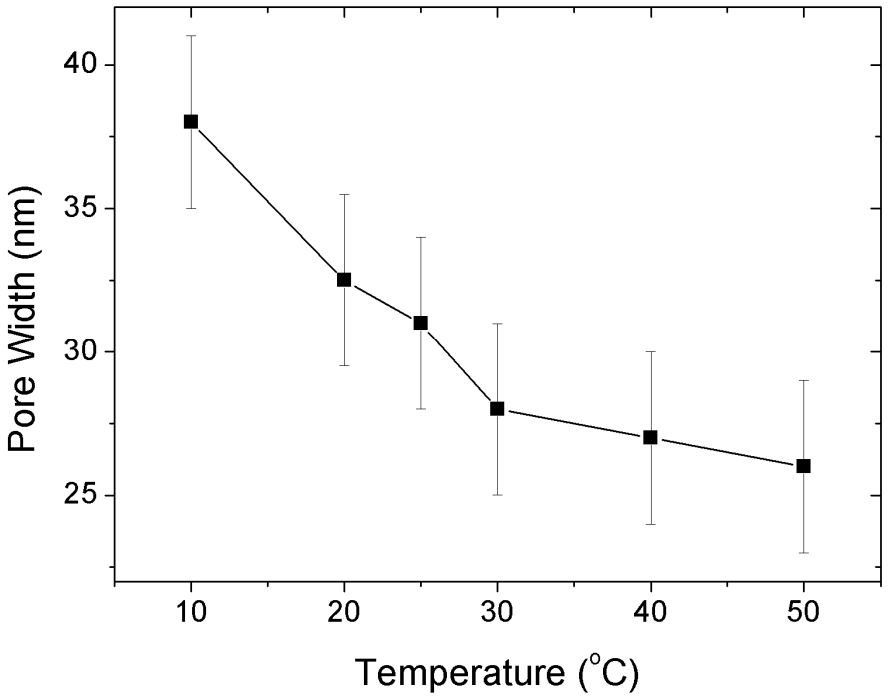


Figure 4. Plot of pore width against temperature for porous InP layers formed by LPS at 2.5 mV s^{-1} in 9 mol dm^{-3} KOH. Carrier Concentration was ~5.3×10^{18}.

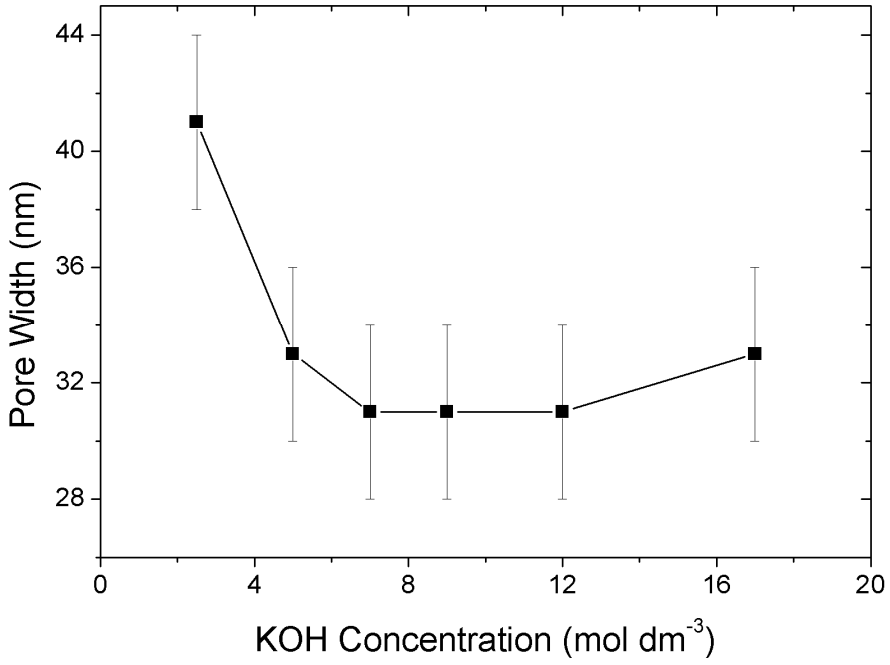


Figure 5. Plot of pore width against KOH concentration for porous InP layers formed by LPS at 2.5 mV s^{-1} at 25°C. Carrier Concentration was ~5.3×10^{18}.

While pore width clearly varies with current density, the majority of the variation occurs at low current densities. Above 5 mA cm^{-2} the variation of pore width with current density is insignificant. As can be seen in Fig. 1, the current densities achieved in a typical LPS are much greater than 5 mA cm^{-2}. In fact, only a small portion (typically <10%) of the charge passed during porous layer formation by LPS is passed at current

densities <5 mA cm^{-2}.[40] This is particularly true for InP with a carrier concentration of ~5.3 x 10^{18} cm^{-3} which was the carrier concentration of all samples anodised at different temperatures and KOH concentrations (and, as can be seen in Fig.1, shows a particularly sharp increase in current at the beginning of porous layer formation). Furthermore, these low current densities occurred at the beginning and end of porous layer formation, and these regions of the porous layer are typically avoided when taking measurements of pore width. Therefore, it is unlikely that the variation in current density observed during the formation of porous InP layers at different carrier concentrations, temperatures and KOH concentrations was responsible for the pore width variation seen in Figs. 3-5.

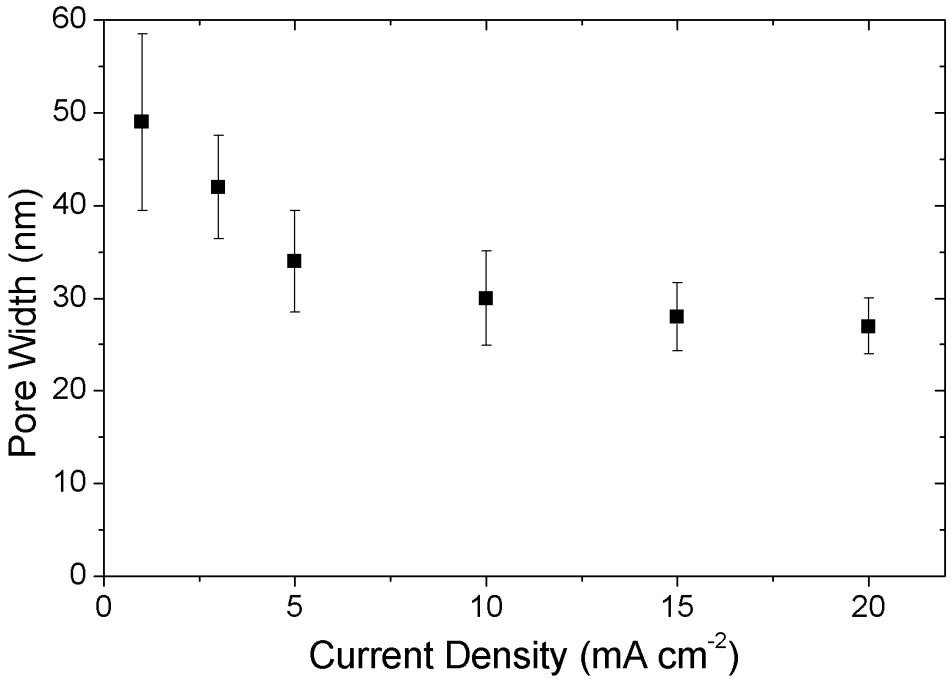


Figure 6. Plot of pore width against current density for porous InP layers formed galvanostatically in 5 mol dm^{-3} KOH at 25°C. Carrier Concentration was ~5.3 × 10^{18}.

Any model which aims to describe the pore formation process will simultaneously have to explain the variation of pore width with temperature, KOH concentration and carrier concentration at high current densities, as well as the variation of pore width with current density that is seen at lower current densities.

Model of Pore Formation

To explain the variations in pore width we invoke a mechanism for pore formation which is based on the competition in kinetics between hole diffusion and electrochemical reaction at the pore tip.[40] In this mechanism, pore formation is said to involve three important steps. A schematic of these three processes is shown in Fig. 7. The first step is the supply of holes to the semiconductor surface which is typically rate limiting for the anodic etching of n-type semiconductors. In the absence of light, holes must tunnel across the depletion layer at the surface in order to take part in the reaction there. In some regions of the surface, the depletion layer thickness x_{sc} will be lower (*e.g.* due to the presence of a defect) and as a result, etching will commence at that site preferentially. As an etch pit is formed at that site, the surface curvature inside the pit will be greater than the curvature at the planar surface. This curvature will tend to increase the electric field at

the base of the etch pit,[44] locally decreasing depletion layer width and leading to preferential hole supply at that site. If the supply of holes were the only factor affecting the etching process then you would expect that the etch front (pore tip) would wander down into the substrate, loosely following the direction of hole supply. The observation of crystallographically oriented etching suggests that other mechanisms must dictate where exactly the reaction takes place.

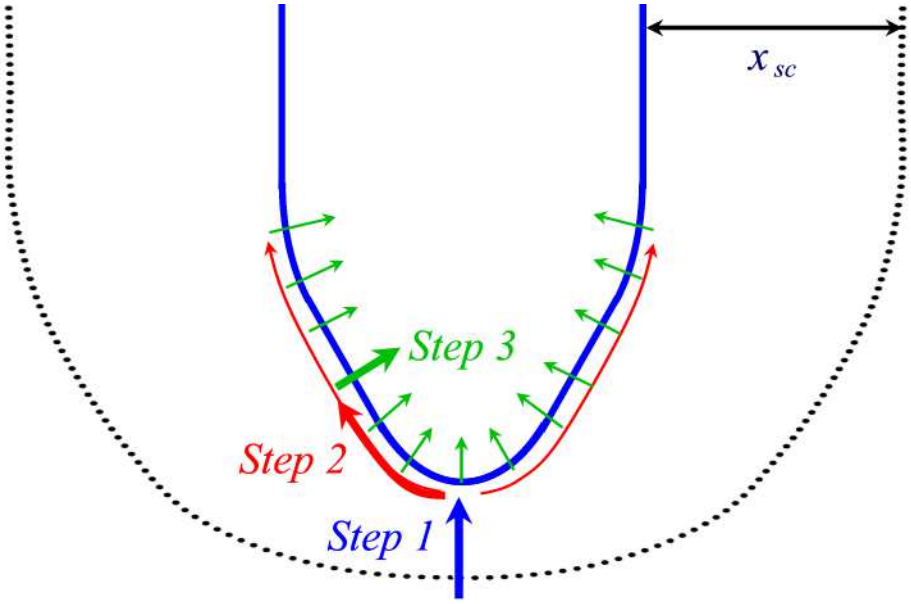


Figure 7. Schematic representation of the three-step etching mechanism at a pore tip. Step one is the tunnelling of holes across the space charge layer (of thickness x_{sc}) which can occur only at the pore tip. Step two is the diffusion of holes at the electrode surface, away from the pore tip. The third step is the oxidation of the semiconductor in the electrochemical reaction.

Once the holes are generated at the electrode surface, they must have some time to diffuse at the surface, before taking part in the electrochemical reaction. The diffusion of holes at the surface, and their annihilation in the electrochemical reaction are the second and third steps in the pore formation mechanism, respectively. This diffusion step is necessary to allow holes to react at preferential etching sites (leading to crystallographic etching) and not just at the pore tip.

Factors Affecting Pore Width

In our model, the width w_p of a pore is determined by the width w_t of the tip (Region 1 in Fig. 8) and an additional width Δw due to diffusion of holes before reaction, *i.e.* $w_p = w_t + \Delta w$ (see Fig. 8). The tip width w_t is determined primarily by the radius of curvature at which the electric field reaches the threshold for hole generation and this depends primarily on the thickness of the depletion layer.[4, 44] Thus w_t is not expected to vary significantly for a given carrier concentration. Since Δw depends on the diffusion distance of holes, it is predicted to increase with faster diffusion but to decrease with faster electrochemical reaction. An increase in temperature should increase the rate of electrochemical reaction more than the rate of diffusion since the activation energy for reaction is expected to be significantly larger than the activation energy for diffusion.

Consequently, with increasing temperature the diffusion distance of holes, and therefore the pore width, should decrease as has been shown in Fig. 4.

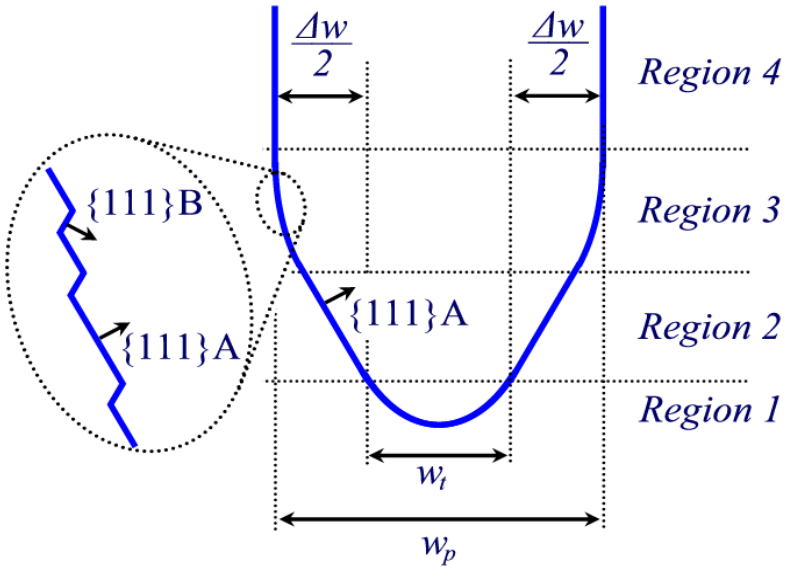


Figure 8. Schematic representation (not to scale) of the different regions of the pore. Region 1 is the high curvature region where hole generation occurs. Region 2 consists of three {111}A facets and Region 3 is intermediate between Region 2 and the pore walls (Region 4). In Region 3, the surface of the pore is stepped as shown in the inset and curves away from the {111}A facets as etching slows. No etching occurs in Region 4

In a similar manner, increasing the concentration of the electrolyte is likely to increase the kinetics of the electrochemical reaction, up to a point. As the solution becomes more concentrated, its structure may change significantly. For example, the variation of conductivity with KOH concentration shows a maximum at around 7 mol dm^{-3} decreasing as concentration is further increased.[51] It is therefore reasonable to expect that the kinetics of the electrochemical reaction will be at a maximum at intermediate KOH concentrations. Since our mechanism predicts a minimum in pore width when electrochemical kinetics are at a maximum, this would lead to thinner pores at intermediate KOH concentrations, with wider pores seen at both higher and lower concentrations. This is precisely what was shown in Fig. 5.

As we suggested earlier, the reduction in pore width with increasing carrier concentration can be explained by considering the effect on both w_t and Δw. As already discussed, the tip width w_t is determined primarily by the thickness of the depletion layer x_{sc}. Since the value of x_{sc} at a given potential decreases with increasing carrier concentration, the radius of curvature of the pore tip must also decrease. This would lead to a decrease in pore width with increasing carrier concentration. The value of Δw may also be affected by the thinner depletion layer. The model of Ostermeyer *et al.*[52] for hole diffusion and annihilation by electrochemical reaction during photoanodic etching showed that when holes are confined in a thinner near-surface region, their diffusion distance is shorter. Furthermore, as described by Blakemore,[53] impurity scattering associated with increased doping also significantly decreases the mobility of holes for dopant concentrations of greater than 10^{16} cm^{-3}. Thus, the thinner diffusion layer and greater scattering of carriers at higher carrier concentrations could decrease Δw. The model therefore, predicts that pores will be thinner at higher carrier concentrations due to

the decrease in both w_t and Δw with increasing carrier concentration. This is exactly what was demonstrated in Fig. 3.

In summary, the minimum pore width is defined by the width of the pore tip which is in turn determined by its curvature r_0 which depends on x_{sc}. In this sense, the InP carrier concentration determines the minimum pore width. The pore width can be greater than this if conditions (e.g. slow electrochemical kinetics) allow the holes to diffuse along the surface, away from the pore tip. Furthermore, as we will explain, this model can also be used to explain why, as shown in Fig. 6, increasing current density causes an asymptotic decrease in pore width to a characteristic pore width that is dependent on x_{sc}.

Crystallographic Etching Mechanism and the Variation of Pore Width with Current Density

In order to understand the variation of pore width with current density, we must first consider the crystallographic etching mechanism in more detail. When the kinetics of Step 3 are sufficiently slow that holes can diffuse to crystallographically preferred reaction sites, etching will eventually reveal the slowest etching crystal facets – the {111}A facets.[54] These {111}A planes are terminated by indium atoms, each bonded to three underlying phosphorus atoms. Removal of an indium atom therefore exposes three phosphorus atoms, each with a dangling bond[33, 54] as shown in Fig. 9. Such a phosphorus atom is easily etched, breaking a bond to each of three indium atoms, two of which are surface atoms. Each of these now has two dangling bonds (each already had one) and consequently is easily etched, revealing two new phosphorus atoms, each with a dangling bond.

Phosphorus atoms with single dangling bonds can be considered to be part of a {111}B surface oriented normal to the bonds.[55] Thus, the removal of a single indium atom from a {111}A surface creates three monatomic ledges with {111}B faces. Etching of the phosphorus atoms on these ledges, and the associated indium atoms, causes the ledges to advance, consequently increasing the size of the three sided region where the next underlying {111}A plane is exposed. New vacancy sites are not formed easily but, once formed, they expand by rapid two-dimensional etching along the surface to expose the next {111}A plane. Eventually, an indium vacancy forms in the newly exposed {111}A face and the etching process continues to expose the next underlying {111}A plane (see Fig. 9). Thus, in the vicinity of the pore tip, the {111}A faces are etched, one monolayer at a time. Symmetrical etching of the three {111}A faces forming the tip causes it to propagate in the (fourth) <111>A direction.[33]

At low current densities, once the initial indium vacancy is created, the low rate of hole supply will ensure that there is little competition for the rapidly etched phosphorus atoms on a {111}B ledge and it is likely that most etching will occur at these favoured sites resulting in the lateral expansion of the void (see left hand side of Fig. 10) as described in the crystallographic etching mechanism. The void will continue its outward expansion in two dimensions until either the rate of hole supply changes or the distance between the pore tip and the back wall of the facet exceeds the effective diffusion length of holes at the InP surface (*i.e.* $\Delta w/2$ in Fig. 8). At a constant current, the rate of hole supply should not change significantly and so the pore widening (by Δw) will approach its theoretical maximum for those conditions (i.e. temperature, KOH concentration) which is defined by the effective diffusion length of holes at the InP surface. These wide pores should also have smooth pore walls and a crystallographically defined pore tip due to the preponderance of etching at crystallographically favoured sites.[50]

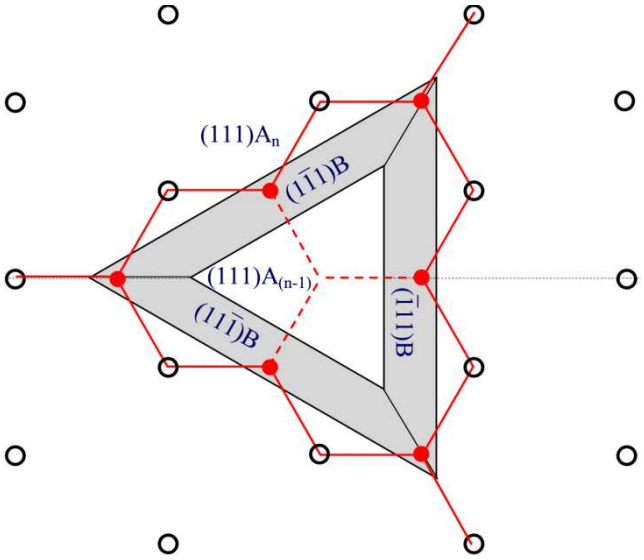


Figure 9. An In vacancy (○) on a {111}A surface creating three dangling P bonds (▮▮▮▮▮). These P atoms (●) correspond to a {111}B monatomic ledge on three sides of the vacancy (projections of which on the {111}A plane are shown). Indium atoms are shown as open circles (○).

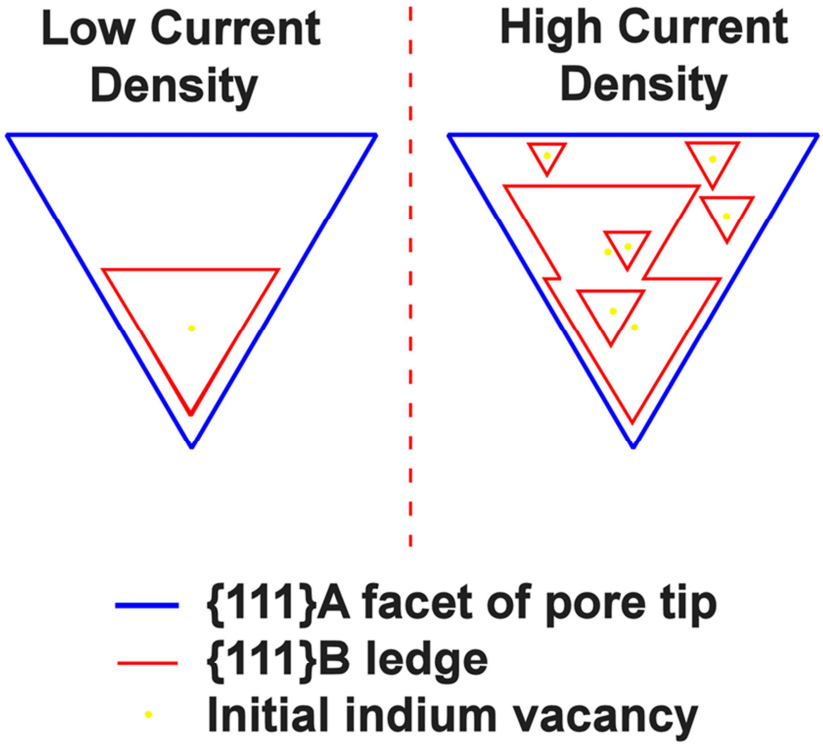
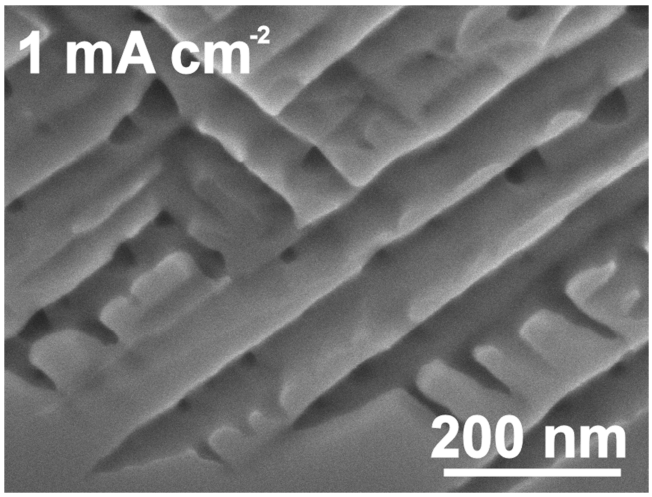
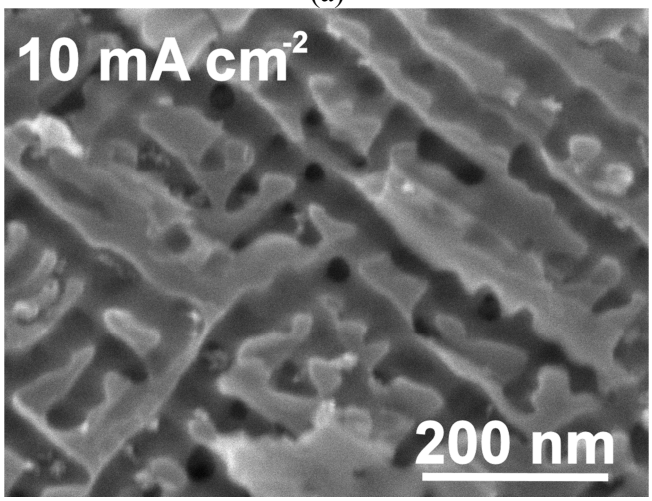


Figure 10. Schematic for the effect of current density on the crystallographic etching mechanism. At low current densities, preferential etching of {111}B ledges leads to the expansion of the voids near the pore tip, favouring pore widening over pore propagation. At higher current densities, the relative increase in competition for favourable etching sites leads to the formation of many more voids, favouring pore propagation over pore widening

At higher current densities, the competition for the rapidly etched sites on the {111}B ledges is higher due to the relative abundance of holes on the surface. This will increase the likelihood of etching another indium vacancy within the existing void (see right hand side of Fig. 10). This results in the formation of many voids on {111}A facets, which increases the number of fast etching {111}B ledges in the vicinity of the pore tip. These fast etching sites will tend to capture more holes near the pore tip and as a result, most of the etching takes place near the pore tip (*i.e.* Δw is relatively small) at higher current densities, resulting in narrower pores. In this sense, the current density can also be said to limit the effective diffusion length of holes at the InP surface, and hence limit Δw, in a similar manner to the kinetics of the electrochemical reaction. Due to the increased etch rate near the pore tip, pores formed at higher current densities should also exhibit rougher walls and have a much less crystallographically defined cross-section than those formed at lower current densities.



(a)



(b)

Figure 11. Cross Sectional SEM micrographs of the $(0\overline{1}\overline{1})$ plane of an n-InP sample galvanostatically anodised at (a) 1 mA cm^{-2} and (b) 10 mA cm^{-2} in 5 mol dm^{-3} KOH. The pores formed at low current density show crystallographically defined pore walls (smooth walls with triangular cross sections) while the pores formed at higher current densities show rougher walls and rounded cross sections.

Figure 11 shows high resolution SEM micrographs of pores and their tips, formed at (a) low (1 mA cm^{-2}) and (b) high (10 mA cm^{-2}) current density. The pores formed at low current density do indeed show smooth pore walls and sharp pore tips as expected. The pore cross-section can also be seen by looking at the pores which are propagating through the plane of the image, and appear as dark features, typically within other pores. These pore cross sections are roughly triangular, being defined by three {112} planes.

The pores formed at 1 mA cm^{-2} are also clearly very wide, with thin pore walls. This is to be expected from the diffusion of holes away from their source at the pore tip, leading to etching in extreme proximity to a neighbouring pore. Holes could not have been supplied to this inter-pore region by tunnelling due to the overlap of the depletion layers of the neighbouring pores. This effectively defines a depletion width of $2x_{sc}$ between the pores which is too large for significant tunnelling to occur.

The well-defined pore morphology seen at 1 mA cm^{-2} (Fig. 11a) contrasts with the much rougher appearance of the pore walls formed at 10 mA cm^{-2} (Fig. 11b). The pore cross-section (again visible as dark features for pores passing through the plane of the image) is also clearly less structured, appearing rounded. This suggests more homogenous (*i.e.* less crystallographic) etching has occurred at the higher current density as predicted by our model. The pore wall thickness is also much greater, indicating that holes did not diffuse as far from their source at the pore tip at higher current densities. Since no holes can be supplied to the pore walls by tunnelling (due to the overlap of depletion layers of neighbouring pores) or by diffusion from the pore tip, thicker pore walls resulted.

Conclusions

InP porous layers formed anodically in KOH exhibit significant pore width variations. The pore width is related to the InP carrier concentration, current density, temperature and electrolyte concentration. These variations in pore width can be understood within the framework of a three-step model for pore formation in InP. The first step is hole supply to the semiconductor surface which occurs by tunnelling due to the curvature enhanced electric field at the pore tip. The second step is the diffusion of holes at the semiconductor surface, away from the pore tip. The third step is the actual electrochemical reaction. The minimum pore width is determined by the carrier concentration, which defines the shape and extent of the pore tip. Pores can be widened by the diffusion of holes away from the pore tip before reaction. The competition in kinetics between the diffusion of holes at the surface and their annihilation in the electrochemical reaction is what determines the final pore width.

The decrease of pore width with increasing carrier concentration is explained in terms of its influence on step one. At higher carrier concentrations, the thinner depletion layer leads to a sharper pore tip and more spatially confined hole supply which limits the extent of etching. The low pore widths measured at high temperatures and intermediate KOH concentrations is explained in terms of the increased electrochemical reaction kinetics, which limits the effective diffusion distance of holes at the surface which again limits the spatial extent of etching.

The variation of pore width with current density is also explained within the framework of the model by considering the crystallographic etching mechanism. It is shown that the pore width variation with current density is also due to a change in the effective diffusion length of holes at the surface. This model is supported by observation

of the different crystallographic features of the pore cross section at different current densities.

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